Abstract of the Invention

There is disclosed a digital filter or a receiver including a digital filter having at least two multiple stage shift registers. A plurality of multipliers corresponding in number to the number of stages in the at least two multiple stage shift registers receive as a first input an output from a corresponding stage of the at least two multiple stage shift registers. A tap weight shifter is coupled to a tap weight source to receive tap weights. The tap weight shifter is coupled to provide a second input to each multiplier. Each multiplier produces an output that is the product of inputs thereto. An adder sums the multiplier outputs to provide a sum output. The tap weight shifter then circularly shifts the tap weights and another multiply-add operation occurs. Several shift/multiply/add cycles may occur before data is again shifted into the at least two multiple stage shift registers, and another multiply-add operation occurs.